PIN REORDERING DURING PLACEMENT OF CIRCUIT DESIGNS

ABSTRACT

A method (400) of placing a circuit design can include the steps of identifying topological levels of a circuit design representation (415) and determining an arrival time for each input signal to a look up table within a circuit design representation (420). The propagation delay associated with each pin of the look up table can be identified (420) such that the input signals of the look up table can be ordered according to the arrival times of each input signal and the propagation delay of each pin of the look up table (435). The method can continue processing each look up table of an identified topological level (440) as well as each topological level of the circuit design representation (455).